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In the claims:

1. (Original) In a 1394-compliant system of node devices in communication over a distributed bridge, a method of synchronizing cyclemasters over a distributed bridge, the method comprising:

a local portal sending a synchronization signal to a peer portal through a bridge fabric upon occurrence of a cycle synchronization event on the local portal;

the peer portal sampling its local cycle timer to obtain a sample value when the peer portal receives the synchronization signal;

a bridge manager at an upstream portal communicating the sample value to a bridge manager at an alpha portal;

the bridge manager at the alpha portal using the sampled time value to compensate for delays through a bridge fabric, calculate the correction to be applied to a cycle timer associated with the alpha portal, and correct the cycle timer.

- 2. (Original) The method of claim 1, wherein the cycle synchronization event comprises a cycle offset value rolling over.
- 3. (Original) In a 1394-compliant system of node devices in communication over a distributed bridge, a method of synchronizing cyclemasters over a distributed bridge, the method comprising:

connecting an output signal means from a first portal with an input signal means of a second portal and connecting an output signal means from a second portal with an input signal means of a first portal;

sampling the output signal means of the first portal and storing the sampled value;

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communicating the sampled value to a downstream portal; and

the downstream portal adjusting its cyclemaster in response to the sampled

value.

4. (Original) The method of claim 3, further comprising generating an

interrupt when the output signal means is sampled.

5. (Original) The method of claim 3, wherein the sampled value is

communicated to the alpha portal.

6-9. (Cancelled)

10. (Original) A bridge link device, connectable within a 1394-compliant

serial bus architecture, the bridge link device comprising:

a first sampled value reflecting an output signal value;

a second sampled value reflecting an input signal value;

a sample value register, the sample value register containing the first

sampled value and the second sampled value, the sample value register in

communication with software that communicates the sampled values to a downstream

node device.

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